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Wideband CDMA Acquisition System Effects on  
Handset Power Consumption

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## Executive Summary

The 1999 version of the physical layer specification of the IMT2000 standard is complete. Major telecommunication manufacturers are now designing the next generation of cellular communications devices with initial introduction of products and services slated for the year 2001.

The consumer-oriented nature of IMT2000 products places a premium on the communication system performance as well as on other factors of importance to consumers, including handset standby time. Golden Bridge Technology, Inc., has developed a body of unique MATCHED FILTER based system and device technology that concurrently addresses these requirements. It is shown that matched filter solutions are superior to any solution that relies on CORRELATOR BANK technology.

The handset standby time is shown to increase by factors typically on the order of 300% when correlator banks are replaced by matched filters. In addition, for the special case of the W-CDMA system, the handset standby time is shown to increase by an additional factor of 263% when the TDL matched filter architecture is replaced by the GBT architecture.

## Contents

<b>1</b>	<b>Introduction</b>	<b>5</b>
<b>2</b>	<b>W-CDMA Acquisition System</b>	<b>7</b>
2.1	Two Stage Architecture . . . . .	7
2.2	First Stage Acquisition Strategies . . . . .	8
<b>3</b>	<b>GBT Matched Filter Architectures</b>	<b>11</b>
3.1	General Matched Filter Architecture . . . . .	11
3.2	PSC Matched Filter Architecture . . . . .	16
<b>4</b>	<b>Numerical Results</b>	<b>18</b>
4.1	TDL versus Correlator Bank Architectures . . . . .	18
4.2	GBT versus TDL Matched Filter Architecture . . . . .	20
4.3	GBT Matched Filter Architecture for W-CDMA PSC . . . . .	22
<b>5</b>	<b>Conclusions</b>	<b>23</b>
<b>A</b>	<b>TDL and Correlator Power Consumption</b>	<b>25</b>
A.1	The TDL Matched Filter Architecture . . . . .	25
A.2	The Correlator Architecture . . . . .	28

## List of Figures

1	Two-Stage Acquisition Concept . . . . .	8
2	Matched Filter Block Diagram . . . . .	12
3	GBT Matched Filter Block Diagram . . . . .	14
4	Power Consumption Increase Factors, TDL System Reference	19
5	Handset Standby Time, TDL System Reference . . . . .	20
6	GBT MF and Handset Power Reduction, TDL System Reference . . . . .	21
7	GBT MF Handset Standby Time Increase, TDL System Reference . . . . .	22

8	Detailed Matched Filter Block Diagram . . . . .	25
9	Correlator Block Diagram . . . . .	28

## List of Tables

1	Modified TDL Architecture State and Outputs . . . . .	17
2	Gate Counts of Standard Circuit Components . . . . .	26

## 1 Introduction

Spread spectrum communications rely on a spreading code to perform the 'spectral spreading' function. The receiver cannot correctly detect the transmitted data unless: a) it has knowledge of the spreading code and b) has synchronized its locally generated code replica to the received code. Item a) is clearly a function outside of the scope of the (normal) receiver operation; the receiver will have knowledge of the spreading code used at the transmitter if it is intended to receive the signal. Item b) however is a function performed at the receiver. A spread spectrum system that has acquired the incoming signal will generate its local replica of the spreading code in exactly the same phase as the code embedded in the incoming signal.

How well the signal synchronization function is performed at the receiver has significant implications, as will be shown in the sections that follow.

Different design requirements can, and do, influence the architecture of the acquisition system. These requirements may relate to device cost, to the length of time that a signal is transmitted or to other system or user requirements. Many acquisition system designs have emerged over the years, and many have been documented in the open literature.

The subject of this paper is the acquisition of direct sequence spread spectrum (DSSS) signals, in particular as they are designed for the IMT2000 Wideband CDMA (W-CDMA) system. A general classification of the many schemes proposed for DSSS signal acquisition in the open literature over the years can be found in [Simon], which addresses the subject of matched filters and correlators in the context of acquisition systems. Matched filters are described as *high decision rate detectors*, while active correlators are *low decision rate detectors* [Simon, volume III, page 5] since matched filters generate statistics related to the state of offset between the local and incoming spreading codes at the chip rate while correlators generate the same statistics at significantly lower rates.

There is certainly a degree of attractiveness in a high decision rate detector, or matched filter, because it can be intuitively said that it has the potential to significantly speed up the acquisition process. The correlator however is a proven device used in the acquisition systems of many documented designs, both military and commercial. Perhaps the best known design to use a correlator based acquisition system is the IS95 system introduced by Qualcomm. The proven nature of correlator based acquisition system designs, together with the much simpler architecture and the lower power consumption *of an*

*individual device* forms, at least superficially, a compelling argument in favor of using one of the many documented correlator based acquisition schemes.

The argument often made is that the low complexity and power consumption of the correlator makes possible DSSS acquisition system architectures employing multiple correlators operating in parallel, i.e., correlator banks, the decision rates of which can be substantially increased over that of a single correlator. While the power consumption and complexity of a correlator bank also increases in proportion to the number of correlators used, it is perceived to remain substantially lower than that of a matched filter.

The above argument summarizes the thinking of many who believe that the correlator bank represents the best compromise between acquisition system performance and low handset power consumption. The analysis presented in this paper shows that for the W-CDMA system parameters the matched filter is the device of choice, offering the best system acquisition performance and lowest handset power consumption. This analysis also goes on to show that the specific matched filter architecture used is also important to the ultimate handset standby performance. Specifically, the GBT matched filter architectures described in [Tran, Davidovici] are shown to reduce the standby power consumption of *any* handset to 58% of the power consumption obtained using a Tapped Delay Line (TDL) matched filter architecture. For the special case of an IMT2000 W-CDMA handset, the power consumption is reduced to 38% of the power consumption obtained using a TDL matched filter architecture.

The paper is organized as follows: the general acquisition system architecture of the W-CDMA system is described together with applicable signal search strategies. The performance of both matched filters and correlators when implementing these search strategies is addressed. A discussion of the general TDL architecture and applicable methods of power consumption reduction follows. The general case, *i.e.* entirely random acquisition signal, is discussed as well as the special case of the specific W-CDMA acquisition signal, which has a degree of structure that departs from randomness.

The numerical results section uses the results obtained in the previous sections together with the relative power consumption numbers obtained in the appendix to quantify and illustrate the main results. The principal results presented are the degrees of improvement in power consumption obtained by replacing correlators with matched filters, followed by the degrees of improvement obtained by replacing TDL matched filters with Golden Bridge Technology matched filters.

The results show that handsets that use matched filter always have significantly greater standby times than handsets that use correlators. The increase in handset standby time is shown to be on the order of 300% when replacing a correlator based system with a TDL matched filter based system. An additional increase in handset standby time on the order of 160% is obtained when the TDL matched filter is replaced with the GBT enhanced matched filter. For the special case of the W-CDMA signal, the increase in standby time becomes on the order of 260%.

## 2 W-CDMA Acquisition System

The cell acquisition process in the IMT2000 (DS) system is typically carried out in three steps: the slot synchronization, the frame synchronization and the scrambling code identification. Each step uses information available from the successful completion of the previous step. For a more detailed description of the three steps required in the cell search process see [RAN 25.214, TS 25.211]. The first step in the cell search process requires the acquisition of the Primary Synchronization Code (PSC) which consists of a random code of length 256 chips transmitted once every 2560 chips [TS 25.211, Section 5.3.3.4]. The lack of prior information and the physical specifications of the Primary Synchronization Channel (PSCH) led many to consider this step to be the most complex of the cell search process. The operational scenario of the W-CDMA system is such that a two stage acquisition system architecture was recommended in the standard publications. The first stage derives initial statistics that are then processed by the second stage. Here we briefly address the two stage architecture and the potential search strategies that may be implemented at the first stage.

### 2.1 Two Stage Architecture

The received signal to noise ratio is sufficiently low so that results obtained from processing one symbol alone are not considered to be sufficiently reliable. In [T1P1/98-044, Section 3.6.4.1] it is recommended that the first step in the cell search process utilize a two stage process with a matched filter in the first stage. Implied in this recommendation is the realization that the timing (or phase) ambiguity is sufficiently large to eliminate the use of a long matched filter, or of a large correlator bank. A block diagram of a two-stage acquisition system as may be used to acquire the PSC is shown in figure 1.

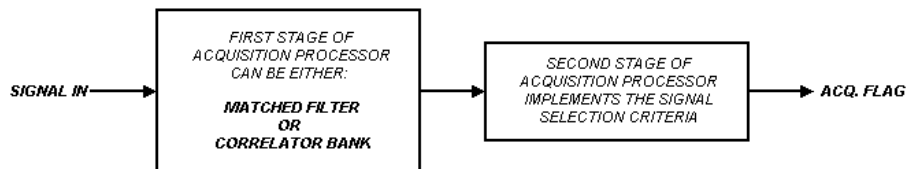


Figure 1: Two-Stage Acquisition Concept

The first stage of the acquisition system correlates the incoming signal and the local replica of the spreading code over a code period duration,  $T_s$ . Two alternative architectures that can implement this function are considered here: a (passive) matched filter and a correlator bank architecture, as shown in figure 1.

A rigorous analysis of the complexity and power consumption of the second stage of the acquisition system for the two potential first stage implementations cannot be performed due to the many possible circuit implementation schemes. It can be said however that the alternative selected for the first stage of the acquisition system greatly influences the complexity of the second stage of the acquisition system. A matched filter, capable of high decision rates, sequentially outputs data at a high but constant rate. The correlator bank produces large amounts of data that occur concurrently, at the end of the integration period. Thus, if a matched filter is used, the second stage of the acquisition system faces the challenge of processing a high speed sequential data stream. If a correlator is used, the second stage of the acquisition system faces the challenge of processing a large amount of bursty data. The challenge of processing data that occurs at a constant rate is generally considered to be preferable to the alternative of processing large quantities of bursty data.

This general conclusion, that the matched filter is a preferable alternative to the correlator bank, will be shown to be in agreement with the quantitative analysis of the performance of the correlator and matched filter bank architectures.

## 2.2 First Stage Acquisition Strategies

The acquisition system shown in figure 1 is a two stage acquisition system. The first stage may consist either of a matched filter or of a correlator bank. The second stage consists of a post-processor that makes acquisition deci-

sions based on the first stage outputs. The structure of the signal described in [TS 25.211, Section 5.3.3.4] requires that the first step of the cell search process examines a timing uncertainty range of at least one slot, which is  $N = 2560$  possible relative phase alignments.

More than one search strategy can be applied to the acquisition process. One possible strategy is the maximum likelihood (ML) strategy, which examines the correlations of the two signals for all possible phase alignments prior to making any decision. This requires the computation of  $N$  correlations per slot, using a search phase step of one chip. The matched filter is a high processing rate device and it calculates one such correlation in  $T_c$  seconds, following the initial loading. The complete set of correlations therefore require  $T_{MF} = PG \times T_c + (N - 1) \times T_c$  seconds to complete. In contrast, a single correlator is a low processing rate device and it requires  $T = PG \times T_c$  to complete a single correlation. The entire set of  $N$  correlations is completed in  $T_{1C} = N \times PG \times T_c$  seconds. Grouping  $m$  correlators in a correlator bank has the advantage of increasing the processing rate. The processing time required of an  $m$  correlator bank to perform all  $N$  correlations is  $T_{mC} = PG \times T_c \times \lceil N/m \rceil$  seconds.

Another search strategy may be the Neyman-Pearson (NP) strategy, which minimizes the probability of a missed detection subject to fixing the probability of a false alarm to a desirable value [Simon, Volume III, page 5]. This strategy sets a threshold and declares the phases aligned when the correlation output crosses that threshold. Assuming that a signal is present, and that it will be detected with high probability, the a priori probability of the correlation result crossing the threshold at any given phase alignment is  $P_{gp} = 1/(10 \times PG)$ . The matched filter examines the result of a new correlation every  $T_c$  seconds and if the threshold crossing occurs after the  $i^{th}$  correlation, the total search time is  $t = i \times T_c$  where  $i = 1, 2, \dots, 10 \times PG$ . The average time for the matched filter output to cross the threshold is then found as

$$T_{MF} = \sum_{i=1}^{10 \times PG} i \times T_c \times P_{gp}$$

The single correlator lends itself to a similar analysis, except that the time spent prior to crossing the threshold at the  $i^{th}$  trial is  $t = i \times PG \times T_c$ . Therefore the average time to cross the threshold becomes

$$T_{1C} = \sum_{i=1}^{10 \times PG} i \times PG \times T_c \times P_{gp}$$

It is readily observed from the above that  $T_{1C} = PG \times T_{MF}$ , which is not an unexpected result. The  $m$  correlator bank examines the entire phase uncertainty in groups of  $m$  phases at a time, and thus derives  $m$  statistics during the time required by a single correlator to derive one statistic. The entire phase uncertainty is divided into  $n_g = \lceil 10 \times PG/m \rceil$  groups. The probability of the threshold being crossed at the end of the  $i^{th}$  trial is

$$P_{gp} = \begin{cases} m/(10 \times PG) & \text{for } i = 1, 2, \dots, n_g - 1 \\ 1 - ((n_g - 1) \times m)/(10 \times PG) & \text{for } i = n_g \end{cases}$$

and the average time required for the  $m$  correlator bank to cross the threshold becomes

$$T_{mC} = \sum_{i=1}^{n_g} i \times PG \times T_c \times P_{gp}$$

It is possible to derive figures of merit from the ratios of the processing time required by the matched filter and the  $m$  correlator bank. Two figures of merit can be derived, corresponding to the two search strategies outlined above. Thus,

$$F_{ML} = (PG \times T_c)/(PG \times T_c \times \lceil PG/m \rceil) = 1/\lceil PG/m \rceil$$

$$F_{NP} = \frac{\sum_{i=1}^{10 \times PG} (i \times T_c \times P_{gp})}{\sum_{i=1}^{n_g} (i \times PG \times T_c \times P_{gp})}$$

The results above are not unexpected. The  $F_{ML}$  especially can be interpreted to indicate that

‘the correlator bank approaches the processing capability of the matched filter in proportion to the number of correlators to the number of stages in the matched filter’

As expected, this also indicates that a ‘full correlator bank’ has the same processing rate as a matched filter.

### 3 GBT Matched Filter Architectures

Golden Bridge Technology has been very active in the design and application of low power matched filter architectures. Two of the most significant improvements are detailed in references [Tran, Davidovici]. Both inventions describe methods of implementing matched filters with novel architectures that significantly reduce the device's power consumption. The first invention, [Tran], addresses the general case, where the spreading signal is random and devoid of any structure that can be used to advantage. The second invention, [Davidovici], addresses the case where the signal, although random, has a degree of structure that can be used to advantage. An example of such a signal is the Primary Synchronization Code (PSC) described in [RAN 25.213, Section 5.2.3.1]. The presence of a degree of structure can be exploited to further reduce the matched filter's power consumption.

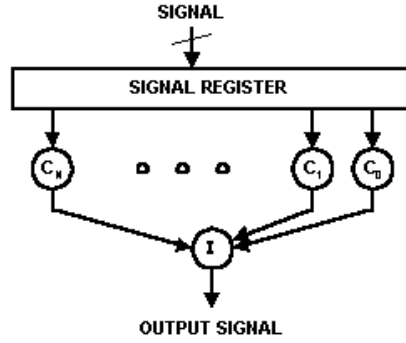
#### 3.1 General Matched Filter Architecture

The matched filter architecture illustrated in figure 2a is the conventional Tapped Delay Line (TDL) architecture. This architecture is easily understood and has been widely used in the literature. The TDL architecture is not however the architecture of choice when implementing power consumption sensitive applications. GBT has developed a novel matched filter architecture that has a much lower power consumption. A detailed public domain description of this architecture can be found in [Tran]. The foundation of the GBT architecture can best be understood by first revisiting the operation of the conventional TDL architecture.

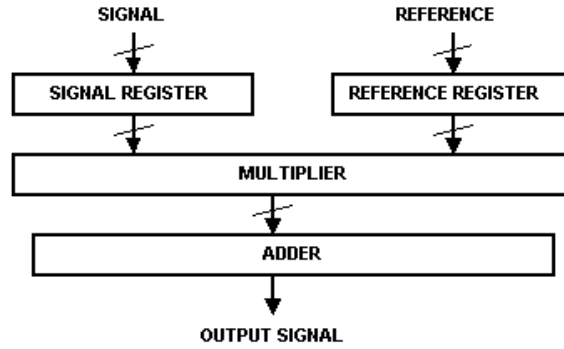
The TDL architecture can be said to perform a dot product between two vectors: the vector that contains the signal samples, and the weight vector that contains the tap coefficients. In this context the weight vector will be referred to as the reference vector since it contains the local spreading code reference, and the TDL architecture of figure 2a can be redrawn as shown in figure 2b. Considering a TDL of  $l_{full}$  stages, the output of the TDL at some time  $k$  is given by

$$T_k = \sum_{i=1}^{l_{full}} s_{i+k} \times r_i$$

where  $s_j, j = 1, 2, \dots$  are the incoming signal samples and  $r_i, i = 1, 2, \dots, m$  are the reference vector elements. For example, let  $l_{full} = 9$  and show the



(a)



(b)

Figure 2: Matched Filter Block Diagram

TDL output at two time instants,  $k = 0$  and  $\ell$ . At the time instant  $k = 0$ ,

$$T_0 = \sum_{i=1}^9 s_i \times r_i = \sum_{i=1}^3 s_i \times r_i + \sum_{i=4}^6 s_i \times r_i + \sum_{i=7}^9 s_i \times r_i$$

Associated with the output at time  $T_0$  define the partial terms above as  $P_1^0, P_2^0$  and  $P_3^0$ , with

$$P_1^0 = \sum_{i=1}^3 s_i \times r_i = s_1 \times r_1 + s_2 \times r_2 + s_3 \times r_3$$

$$P_2^0 = \sum_{i=4}^6 s_i \times r_i = s_4 \times r_4 + s_5 \times r_5 + s_6 \times r_6$$

$$P_3^0 = \sum_{i=7}^9 s_i \times r_i = s_7 \times r_7 + s_8 \times r_8 + s_9 \times r_9$$

At the time instant  $k = \ell$ ,

$$T_\ell = P_1^\ell + P_2^\ell + P_3^\ell$$

and

$$P_1^\ell = \sum_{i=1}^3 s_{i+\ell} \times r_i = s_{1+\ell} \times r_1 + s_{2+\ell} \times r_2 + s_{3+\ell} \times r_3$$

$$P_2^\ell = \sum_{i=4}^6 s_{i+\ell} \times r_i = s_{4+\ell} \times r_4 + s_{5+\ell} \times r_5 + s_{6+\ell} \times r_6$$

$$P_3^\ell = \sum_{i=7}^9 s_{i+\ell} \times r_i = s_{7+\ell} \times r_7 + s_{8+\ell} \times r_8 + s_{9+\ell} \times r_9$$

The partial term based representation above suggests that the partial terms may be calculated *one at a time*. The implications of this simple concept are extremely important since the calculation of a *single partial term* necessitates a smaller signal register and adder tree, therefore resulting in potentially large power savings. For this example, three partial terms are calculated. The signal register is reduced to one third of its original size while the adder tree is reduced to less than one third of its original size. The reference register is divided in three sections, each being switched-in by the multiplexer.

The calculated partial terms must be stored since, for this example, three partial terms are required for each matched filter output. The storage memory however consumes much less power than the signal register and adder tree segment that it replaces, thus creating a significant overall power saving. As an operational example, consider how a modified TDL structure capable of calculating only one partial term at a time may replace the operation of the full TDL structure above. The steps of the algorithm for building this modified TDL structure are listed below while the block diagram of the device is illustrated in figure 3:

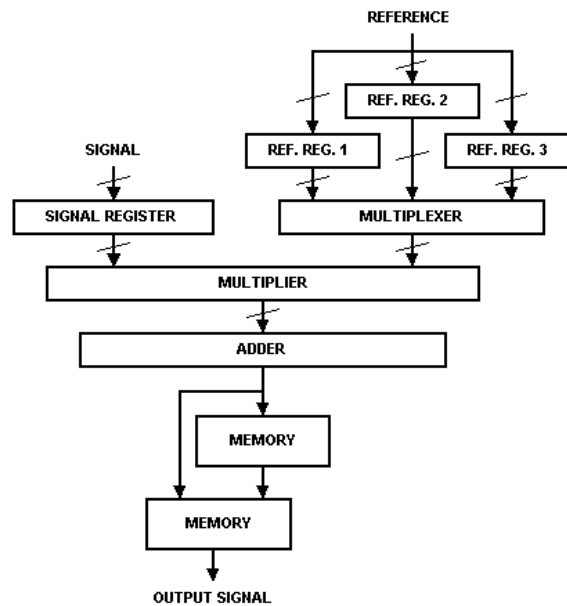


Figure 3: GBT Matched Filter Block Diagram

1. Reduce the input signal register and the associated multiplier and adder tree of the TDL structure to one-third of its original size.
2. Separate the reference register into three segments. For this example, the original reference register length was  $l_{full} = 9$  and the length of each segment is  $l_{seg} = 3$ . The reference register segment contents are  $R_3 = (r_9, r_8, r_7)$ ,  $R_2 = (r_6, r_5, r_4)$  and  $R_1 = (r_3, r_2, r_1)$ .
3. Introduce a multiplexer between the reference register and the multiplier that it connects to. The multiplier has the capability to connect either of the three reference register segments to the multiplier.
4. Introduce a memory block at the output of the adder tree. The memory block will store some of the partial terms.
5. Introduce a final adder between the memory block output and the adder output. The output of this final adder is the output of the TDL matched filter.

The operation of the modified TDL architecture consists of the following steps:

1. Shift a new sample into the reduced length signal register. For this example, the original length was  $l_{full} = 9$  and the reduced length is  $l_{seg} = 3$ .
2. Correlate (perform the dot product) with each of the three reference register segments, in turn. Assume the signal in the shift register to be  $S_\ell = (s_{3+\ell}, s_{2+\ell}, s_{1+\ell})$ . Using the definitions above, the partial terms generated by correlating with the three reference register segments are:

$$\begin{aligned}
S_\ell \cdot R_3 &= (s_{3+\ell}, s_{2+\ell}, s_{1+\ell}) \cdot (r_9, r_8, r_7) = P_3^{\ell-6} \\
S_\ell \cdot R_2 &= (s_{3+\ell}, s_{2+\ell}, s_{1+\ell}) \cdot (r_6, r_5, r_4) = P_2^{\ell-3} \\
S_\ell \cdot R_1 &= (s_{3+\ell}, s_{2+\ell}, s_{1+\ell}) \cdot (r_3, r_2, r_1) = P_1^\ell
\end{aligned}$$

The three partial terms generated for each new signal sample belong to different signal epochs (*i.e.*, different time instances). The role of the memory is to hold the partial terms generated at each step until all partial terms for a specific signal epoch are available.

3. Retrieve from memory the partial terms required to form the matched filter output and generate the output by summing all three partial terms. At the computational instant above the partial term  $P_3^{\ell-6}$  is summed with the corresponding  $P_2^{\gamma-3}$  generated three computational steps earlier and the corresponding  $P_1^\lambda$  generated six computational steps earlier, which are now retrieved from memory. Accounting for the time epoch of generation, *i.e.*, how many steps earlier the partial terms were generated,  $\gamma = \ell - 3$  and  $\lambda = \ell - 6$ . Thus, the output will be

$$T_{out} = P_1^\lambda + P_2^{\gamma-3} + P_3^{\ell-6} = P_1^{\ell-6} + P_2^{\ell-6} + P_3^{\ell-6} = T_{\ell-6}$$

Table 1 illustrates the operation of the modified TDL architecture. The first column is the time epoch, where each time epoch indicates the introduction of a new signal sample into the modified TDL's signal register. Table 1 covers 11 epochs. The second column illustrates the state of the modified TDL's signal register. Each new epoch the signal register contents are shifted by one and a new signal sample is introduced. Column three represents which segment of the modified TDL's reference register is used for the correlation process. Each epoch all three reference register segments

are used in sequence, generating three partial terms. Column four designates the partial term generated during the correlation of the signal vector with the specific reference register segment. The following columns, labeled 1 through 6, indicate which partial terms ( $P$ ) are combined in order to generate the matched filter's output at that particular instance of time. The last column illustrates which partial terms are summed in order to generate the final matched filter output.

As seen, the first matched filter output is generated by the summing the first partial term at time epoch zero,  $P_1^1$ , to the second partial term at time epoch three,  $P_2^4$ , to the third partial term at time epoch six,  $P_3^7$ . Thus, as shown in Table 1, the sum of the partial terms is

$$T_{out} = P_1^1 + P_2^4 + P_3^7 = T_0$$

The above example used a *reduction factor* of three, *i.e.* the signal register is reduced to one third of its value in the conventional TDL architecture implementation. Using the available 0.35 micron Samsung library the power consumption of this matched filter implementation is 62% of the conventional TDL implementation using the same library. Lower power consumptions are possible when using larger reduction factors. The power consumption drops to 47% of the TDL implementation at a reduction factor of eight and to 41% of the TDL implementation at a reduction factor of 16.

### 3.2 PSC Matched Filter Architecture

The Primary Synchronization Code (PSC) described in [RAN 25.213, Section 5.2.3.1] is built by repeating a short code with overlaid modulation. This structure can be used to advantage to significantly reduce the power consumption beyond what is feasible using the method described above. Specifically, the PSC matched filter can have a two-part structure as described in [Tran], where two matched filters are cascaded in order to realize additional size and power consumption gains made possible by the signal structure.

The first part of the two-part matched filter consists of a TDL architecture matched to the short code while the second part of the two-part matched filter consists of a second TDL architecture matched to the overlaid modulation. The two cascaded TDL are not identical. The first TDL, matched to the short repeating code, is implemented using the conventional TDL architecture. The power consumption of this matched filter can be further

epoch	signal	reference	sum	1	2	3	4	5	6	output
0	$s_3, s_2, s_1$	$r_3, r_2, r_1$	$P_1^0$	x						
		$r_6, r_5, r_4$	$P_2^{-3}$							
		$r_9, r_8, r_7$	$P_3^{-6}$							
1	$s_4, s_3, s_2$	$r_3, r_2, r_1$	$P_1^1$		x					
		$r_6, r_5, r_4$	$P_2^{-2}$							
		$r_9, r_8, r_7$	$P_3^{-5}$							
2	$s_5, s_4, s_3$	$r_3, r_2, r_1$	$P_1^2$			x				
		$r_6, r_5, r_4$	$P_2^{-1}$							
		$r_9, r_8, r_7$	$P_3^{-4}$							
3	$s_6, s_5, s_4$	$r_3, r_2, r_1$	$P_1^3$				x			
		$r_6, r_5, r_4$	$P_2^0$	x						
		$r_9, r_8, r_7$	$P_3^{-3}$							
4	$s_7, s_6, s_5$	$r_3, r_2, r_1$	$P_1^4$					x		
		$r_6, r_5, r_4$	$P_2^1$		x					
		$r_9, r_8, r_7$	$P_3^{-2}$							
5	$s_8, s_7, s_6$	$r_3, r_2, r_1$	$P_1^5$						x	
		$r_6, r_5, r_4$	$P_2^2$			x				
		$r_9, r_8, r_7$	$P_3^{-1}$							
6	$s_9, s_8, s_7$	$r_3, r_2, r_1$	$P_1^6$							
		$r_6, r_5, r_4$	$P_2^3$				x			
		$r_9, r_8, r_7$	$P_3^0$	x						$P_1^0 + P_2^0 + P_3^0$
7	$s_{10}, s_9, s_8$	$r_3, r_2, r_1$	$P_1^7$							
		$r_6, r_5, r_4$	$P_2^4$					x		
		$r_9, r_8, r_7$	$P_3^1$		x					$P_1^1 + P_2^1 + P_3^1$
8	$s_{11}, s_{10}, s_9$	$r_3, r_2, r_1$	$P_1^8$							
		$r_6, r_5, r_4$	$P_2^5$						x	
		$r_9, r_8, r_7$	$P_3^2$			x				$P_1^2 + P_2^2 + P_3^2$
8	$s_{12}, s_{11}, s_{10}$	$r_3, r_2, r_1$	$P_1^9$							
		$r_6, r_5, r_4$	$P_2^6$							
		$r_9, r_8, r_7$	$P_3^3$				x			$P_1^3 + P_2^3 + P_3^3$
10	$s_{13}, s_{12}, s_{11}$	$r_3, r_2, r_1$	$P_1^{10}$							
		$r_6, r_5, r_4$	$P_2^7$							
		$r_9, r_8, r_7$	$P_3^4$					x		$P_1^4 + P_2^4 + P_3^4$
11	$s_{14}, s_{13}, s_{12}$	$r_3, r_2, r_1$	$P_1^{11}$							
		$r_6, r_5, r_4$	$P_2^8$							
		$r_9, r_8, r_7$	$P_3^5$						x	$P_1^5 + P_2^5 + P_3^5$

Table 1: Modified TDL Architecture State and Outputs

reduced using the techniques described above. The second TDL device, matched to the data modulating the short repeating code, processes the output of the first TDL matched filter. Further optimization steps may be applied to it, using methods as described above, resulting in a total matched filter power consumption of less than 11% of the equivalent TDL matched filter architecture.

## 4 Numerical Results

The results presented here address the subject of handset power consumption in the standby mode. It is shown that matched filter based acquisition architectures always perform significantly better in this context than correlator based acquisition architectures. In addition, systems that use GBT enhanced matched filter architectures significantly improve upon this performance.

The numerical development makes the assumption that in standby mode the most demanding function performed at baseband is the neighbor list update that requires at least one signal acquisition. Thus, it is assumed that power consumed during this process represents the power consumption of the entire baseband device to a good degree of approximation. Furthermore, the matched filter is responsible for almost the entire power consumption during the acquisition process, since it is large and processes signals prior to de-spreading, which is the highest rate in the baseband device. For brevity, the ML search strategy results are the ones illustrated. The relative standings of the different architectures are not changed if the results of the NP search strategy were to be the ones illustrated.

The power consumed by the handset is apportioned between the RF receiver (RX) chain and the baseband modem. In standby mode, when acquisition based measurements are the principal tasks performed, this power consumption apportionment is assumed to be 30% RF and 70% baseband. Finally, all numerical results use figures extracted from reference [SAMSUNG].

### 4.1 TDL versus Correlator Bank Architectures

The variable that directly affect the handset power consumption is the acquisition time, which directly affects the power consumed in the RX chain and the power consumption of the first stage of the acquisition system, which may be a matched filter or a correlator bank.

An increase in acquisition time has the effect of forcing the RX chain to be turned on for longer periods of time thus consuming additional battery current, as measured in ampere-hours.

The curve labeled 'CORRELATOR BANK RF NORMALIZED BY TDL RF' in Figure 4 illustrates this effect as the size of the correlator bank, and hence its decision rate, is increased. For a full correlator bank, the curve has a value of one, hence the RX chain does not consume any additional power. As the correlator bank size decreases however so does its decision rate. The acquisition time increases proportionally, which has the effect of forcing the RX chain to stay turned on longer and thus consume additional power. As seen in figure 4a a correlator bank equal to half the number of stages of the TDL requires on the average twice as long to make a decision, hence it forces the RX chain to stay active twice as long and consume twice the power. If the size of the correlator bank is reduced by a factor of two again, the decision rate is also reduced by a factor of two and the power consumption of the RX chain is doubled again.

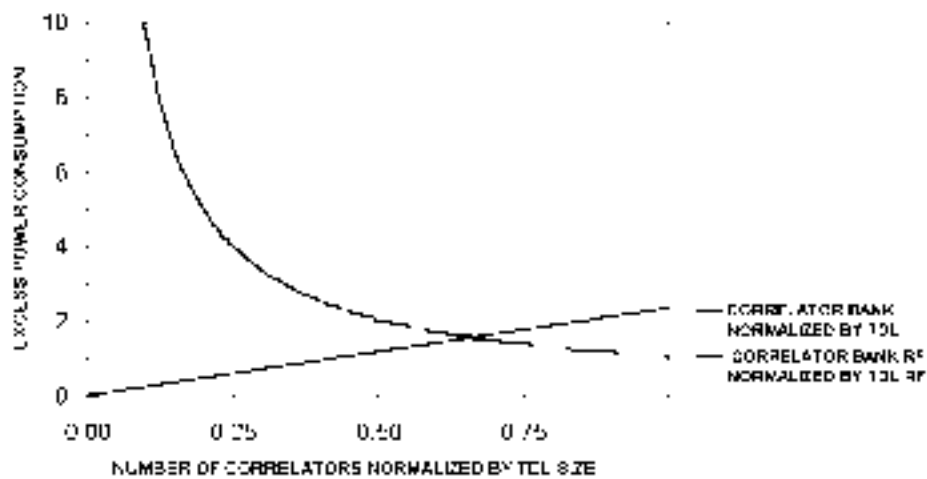


Figure 4: Power Consumption Increase Factors, TDL System Reference

As the correlator bank size increases its power consumption increases as well. As shown by the curve labeled 'CORRELATOR BANK NORMALIZED BY TDL' although a few correlators have a negligible power consumption, a full correlator bank consumes twice the power of the TDL matched filter.

The two power consumption factors combine to illustrate the change in the handset standby time as a function of the size of the correlator bank. As illustrated in figure 5, the standby time of the handset using a correlator bank based acquisition system is approximately one half that of the handset using a TDL matched filter based acquisition system.

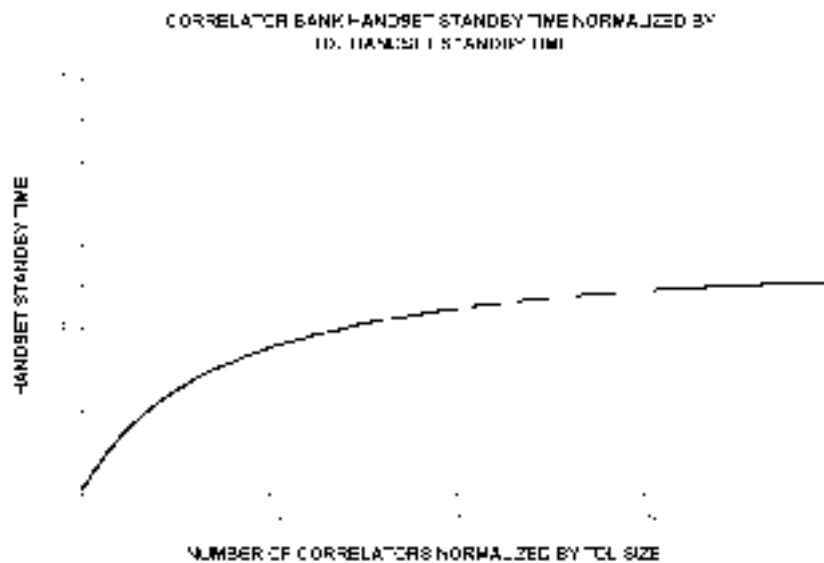


Figure 5: Handset Standby Time, TDL System Reference

## 4.2 GBT versus TDL Matched Filter Architecture

In the previous section it was shown that the matched filter, specifically, the TDL architecture, is always superior to small and medium correlator bank based acquisition system architectures, as it shortens the acquisition time and thus reduces the RX chain power consumption. This reduction is larger than the TDL's increase in its own power consumption as compared to relatively small correlator banks. The net effect of these two factors is an overall reduction in power consumption and an increase in handset standby time. For larger correlator banks, which have decision rates approaching those of the matched filter, their own power consumption also increases, but again the net effect is an overall reduction in power consumption and an increase in handset standby time.

When comparing the effects of the GBT and the TDL matched filter architectures, the decision rates, and thus the acquisition times, are identical. What is not identical is the matched filter power consumption. The reduction of the signal register and adder tree size by some given *reduction factor* and the introduction of memory to hold partial terms has the net effect of greatly reducing the power consumption of the matched filter. Figure 6 illustrates the power saving achievable as the reduction factor is varied from one to 16. At a reduction factor of one the GBT and the TDL matched filter architectures are identical. A reduction factor of two implies that the signal register is one half of its original (TDL) size, a reduction factor of three implies that the signal register is one third of its original (TDL) size, and so on. Of course the memory size increases but the net effect is a reduction in power. As seen in figure 6 the power consumption of the matched filter is reduced to approximately 40% of the corresponding TDL structure at a reduction factor of 16. The corresponding handset power consumption is reduced to approximately 60% of that obtained with the TDL matched filter architecture.

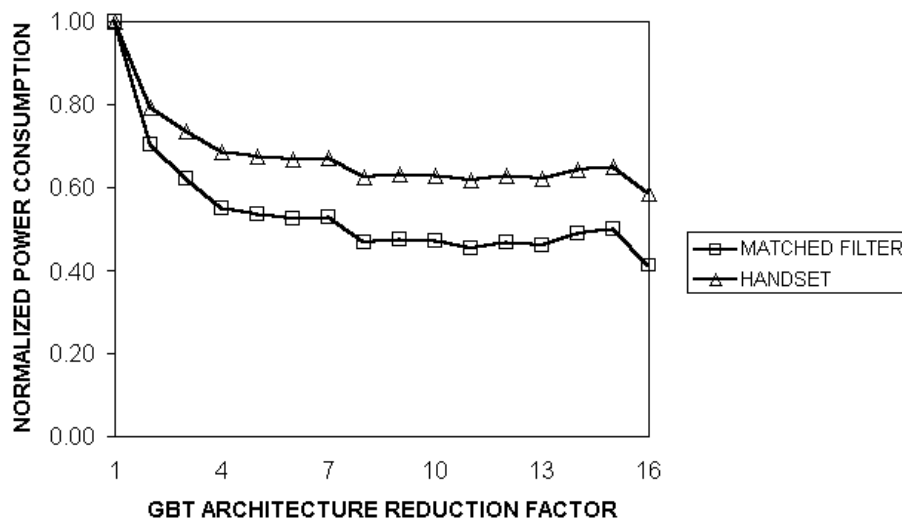


Figure 6: GBT MF and Handset Power Reduction, TDL System Reference

As clearly seen in figure 6 the power reduction curves have an initial steep descent with most of the gains available at a reduction factor of four. Thus

the hardware implementation of this architecture has the potential of being very simple.

The handset standby time is inversely proportional to the power consumption. The potential gains that can be obtained are illustrated in figure 7 for a reduction factor of one to 16.

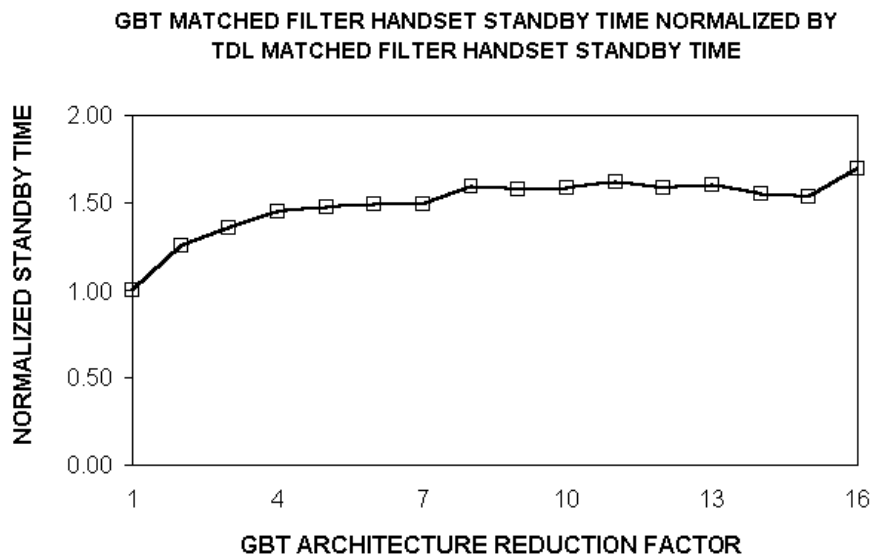


Figure 7: GBT MF Handset Standby Time Increase, TDL System Reference

The benefits to the GBT MF architecture based handset are seen to be substantial, with standby time increases of 146% to 170% over those of the TDL matched filter architecture based handsets, for reduction factors of four to sixteen.

### 4.3 GBT Matched Filter Architecture for W-CDMA PSC

As previously discussed the PSC designed into the W-CDMA has additional structure that can be exploited using techniques discussed in references [Tran, Davidovici]. The application of these techniques yields an additional data point, the power consumption reduction for the GBT designed PSC matched filter architecture compared to the TDL matched filter architecture. The power consumption of the GBT designed PSC matched filter architecture is less than 11% of the TDL matched filter. This results

principally through the application of the two-stage matched filter concept as described in [Davidovici]. Depending on the degree of optimization applied to the first stage above, the power consumption can be further reduced below the 11% figure. The corresponding handset power consumption is reduced to 38% and the standby time is increased to 263% of the TDL based matched filter handset.

## 5 Conclusions

The 1999 version of the physical layer of the IMT2000 standard is now finalized. It describes a cell search process and signal structure that is designed to be used with a two-stage acquisition process. It has been shown that a matched filter based implementation of the acquisition system is superior to any correlator bank based implementation. The handset standby time is doubled when using a TDL matched filter based acquisition system architecture.

It was also shown that Golden Bridge Technology's enhanced matched filter architecture can increase the handset standby times by factors in excess of 170% of the standby times of handsets using TDL matched filter architectures.

For the specific signal structure of W-CDMA PSC signal, further improvements can be made using Golden Bridge Technology's matched filter architectures, such that the handset standby time increases to 263% of that of handsets using TDL matched filter architectures.

## References

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## A TDL and Correlator Power Consumption

The power consumption of the handset is a factor of two elements: the power consumption of the RF and the power consumption of the baseband system. Here it is assumed that the baseband component is the ASIC itself. This is not an unrealistic assumption since it is expected that 0.18 micron VLSI technology has the capability to accommodate the entire W-CDMA modem, including all peripheral functions, within one device. The estimate of the power consumption *ratios* are arrived at indirectly, by the gate count ratios. These are reliable estimates since the TDL and correlator process data at the same input data rate. Furthermore, since it only ratios that are of interest, the results are applicable to any specific technology and library.

### A.1 The TDL Matched Filter Architecture

The VLSI architectures of TDL matched filter is illustrated in figure 8.

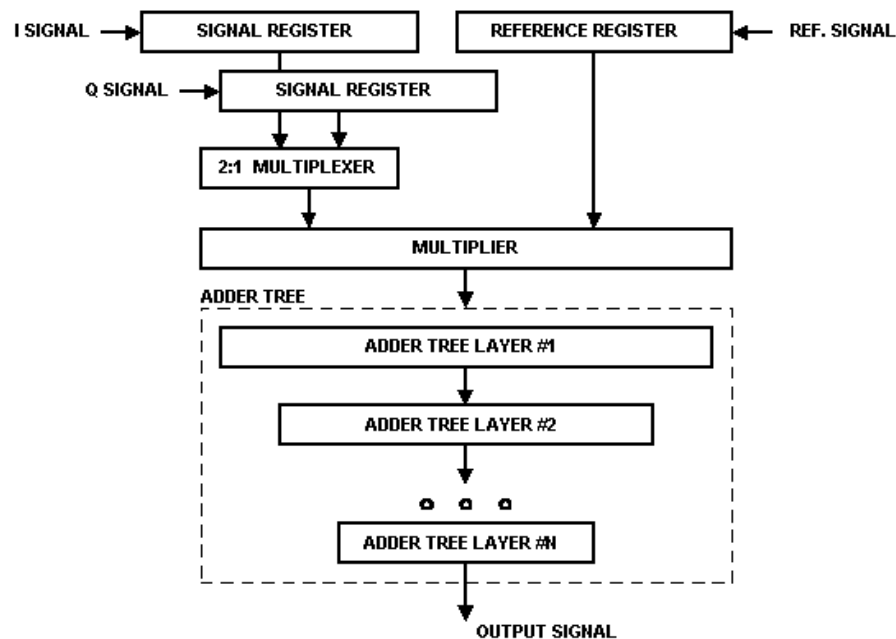


Figure 8: Detailed Matched Filter Block Diagram

The logic elements of the two architectures are registers, multiplexers, mul-

multipliers and adders. These high level components can be constructed using standard VLSI components: flip-flops,  $m$ -bit adders, 2:1 multiplexers (one bit wide) and exclusive-or (XOR) gates. The complexity of these circuit components can be quantized in terms of their 'gate count', or the number of standard gates required for their implementation. Table 2 lists typical gate counts associated with these components.

circuit element	complexity	units
flip-flop	10	gates per flip-flop
adder	10	gates per adder bit
XOR gate	3	gates per XOR gate
MUX (2:1)	3	gates per MUX bit

Table 2: Gate Counts of Standard Circuit Components

The quantization of the TDL matched filter and correlator architectures in units of gates require that dimensions be applied to the building blocks illustrated in figures 8corr block diagram. The following outlines the process used to quantify the above architectures in terms of gate counts.

**Complex shift register.** The incoming signal has an in-phase (I) and a quadrature (Q) component. The matched filter correlates both components with the local replica of the spreading code and  $N_R = 2$  shift registers are required to hold the quantized signal samples. The signal samples are quantized to  $N_{BITS} = 4$  bits and each signal register stores  $PG$  signal samples. The number of bit storage elements, or flip-flops, required for the complex shift register is found from:

$$N_{SR} = N_{BITS} \times PG \times N_R$$

**Reference register.** The samples of the local replica of the spreading code are stored in the reference register. The reference signal samples are quantized to  $N_{RQ} = 1$  bit per sample and the reference register stores  $PG$  signal samples. The size of the reference register is therefore equal to:

$$N_R = PG \times N_{RQ}$$

**Multiplier.** The correlation process requires that the signal samples be multiplied by samples of the local replica of the spreading code. For

the special case in which the local reference code samples are quantized to one bit per sample, the multiplier requires  $N_{XS} = 1$  exclusive-or gates per signal bit. The number of exclusive-or gates in the multiplier is therefore found from:

$$N_{XOR} = N_{BITS} \times PG \times N_{XS}$$

**Multiplexer.** The correlation process involves the operations of multiplication and summation. The large size of the multiplication and summation resources dictates that they be shared, by multiplexing their I and Q inputs. The multiplexer is built-up using one bit 2:1 multiplexer cells. The number of multiplexer cells required is found from:

$$N_{MUX} = N_{BITS} \times PG$$

**Adder tree.** The adder tree is implemented by cascading successive layers of adders. Each adder is capable of adding two inputs and generating one output and the number of adders in adjacent layers is therefore related by factors of two. The number of adders in the first layer of the adder tree is  $N_1 = \lceil PG/2 \rceil$ , the number of adders in the second adder layer is  $N_2 = \lceil N_1/2 \rceil$ , and so on, until the last layer of the adder tree has just one adder. The total number of layers in the adder tree is  $N_L = \lceil \log_2(PG) \rceil$ .

Each adder sums two inputs and generates an output that is one bit wider than the inputs. Thus adders in progressive layers increase in width by one bit. Assigning the adder layers a sequence number,  $1, 2, \dots, N_L$  with the first layer containing the largest number of adders, the width of the  $i^{th}$  layer is found as  $W_i = i - 1 + N_{BITS}$ . The total number of adder-bits in the adder tree can then be calculated to be:

$$N_{AD} = \sum_{i=1}^{N_L} W_i \times N_i$$

The calculations above serve to convert the TDL matched filter architectural components shown in figure 8 into simple circuit elements. Using the figures in Table 2 it is possible to derive the complexity of the TDL matched filter in terms of gates. The TDL matched filter gate count is found to be:

$$MF_G = (N_{SR} + N_R) \times 10 + N_{XOR} \times 3 + N_{MUX} \times 3 + N_{AD} \times 10$$

## A.2 The Correlator Architecture

The correlator architecture, illustrated in figure 9 is much simpler than that of the TDL matched filter.

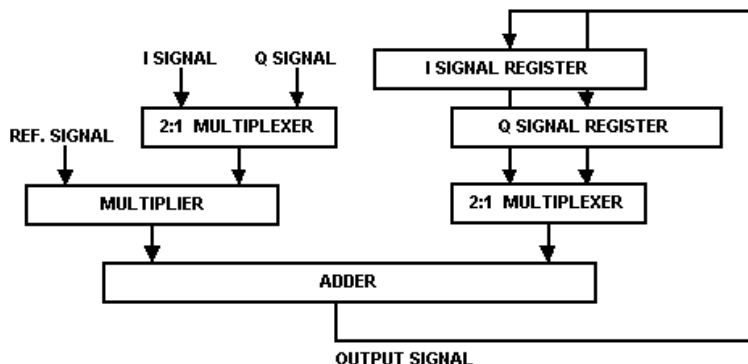


Figure 9: Correlator Block Diagram

It consists of the signal accumulator registers, the multiplexor and the accumulator adder. The complexity of these blocks in terms of simple circuit elements can be shown to be:

**Accumulator adder.** The integration function of the correlator is performed by adding each new product term to the stored summation of previous product terms. The width of the accumulator adder is then

$$N_{AD} = N_{BITS} - 1 + \lceil \log_2(PG) \rceil$$

**Complex signal register.** Two signal registers are required to hold the partial summations of the I and Q signals. The register width is  $N_{AD}$  bits. Thus, the number of storage bits required is

$$N_R = N_{AD} \times 2$$

**Multiplier.** Similar to the matched filter, the multiplier requires  $N_{XS} = 1$  gate per signal bit. The number of exclusive-or gates required for the multiplier is:

$$N_{XOR} = N_{BITS} \times N_{XS}$$

**Multiplexer.** As in the matched filter case, it is effective to time-share the multiplier and adder resources by multiplexing the I and Q input signals. The number of one bit wide, 2:1 multiplexer cells required is:

$$N_{MUX} = N_{BITS} + N_{AD}$$

The gate count complexity of the correlator illustrated in figure 9 is

$$C_G = N_R \times 10 + N_{XOR} \times 3 + N_{MUX} \times 3 + N_{AD} \times 10$$

The gate counts  $MF_G$  and  $C_G$  are indicative of the relative power consumption of the two devices. Specifically, the ratio  $R = MF_G/C_G$  is a good indicator of the TDL matched filter power consumption referenced to a simple correlator.